AF

PATENT
P57002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

TAE-SUNG KIM *et al.*

Serial No.:	10/767,281	Examiner:	WARREN, MATTHEW E.
Filed:	30 January 2004	Art Unit:	2815

For: NOVEL CONDUCTIVE ELEMENTS FOR THIN FILM TRANSISTORS USED IN A FLAT PANEL DISPLAY

TRANSMITTAL OF APPELLANT'S BRIEF FEE

Mail Stop: Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Accompanying this transmittal is an Appeal Brief in support of a Notice of Appeal filed on 11 June 2007. A fee for filing an Appeal Brief has been **previously** paid on **22 November 2006**, together with an Appeal Brief filed on 22 November 2006. The prosecution was **re-opened** prior to a decision on the merits by the Board of Patent Appeals and Interferences on the first Appeal Brief filed on 22 November 2006. In MPEP §1208.02 it is stated that "If prosecution was **re-opened** prior to decision on the merits by the Board of Patent Appeals and Interferences, the fee paid for the Notice of Appeal and Appeal Brief will be **applied to a later appeal on the same application**".

In view of the above, we believe that there is **no fee** incurred by filing this second Appeal Brief. Should any additional fees be incurred, the Commissioner is authorized to charge Deposit Account No. 02-4943 in that amount. Please inform the Applicant of any transactions involving the Deposit Account.

Respectfully submitted,

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Folio: P57002
Date: 7/31/07
I.D.: REB/fw

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

In re Application of:

Appeal No. _____

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APPEAL BRIEF

Paper No. 25

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P.O.Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to Appellants' Notice of Appeal filed on 11 June 2007, Appellants hereby appeal to the Board of Patent Appeals and Interferences from the rejection of claims 1, 2, 4-9, 11-15, 17-19, and 21-24 as set forth in the fourth Office action mailed on 9 March 2007 (Paper No. 20070305).

Applicant previously filed an Appeal Brief on 22 November 2006 and the non-final Office action was issued on 9 March 2007 (Paper No. 20070305) in response to that Appeal Brief. Accordingly, no fee is incurred by filing of the instant Appeal Brief.

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I. REAL PARTY IN INTEREST

Pursuant to 37 CFR §41.37(c)(1)(as amended), the real party in interest is:

SAMSUNG SDI CO., LTD.,
575, Shin-dong
Yeongtong-gu, Suwon-si, Gyeonggi-do
Republic of KOREA

as evidenced by the Assignment executed by the inventors on the 26th of January 2004 and recorded by the U.S. Patent and Trademark Office on the 30th of January 2004 at Reel 014944, Frame 0876.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals and no interferences known to Appellant, Appellant's legal representatives or the assignee which will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 3, 10, 16, and 20 have been canceled. All remaining pending claims 1, 2, 4-9, 11-15, 17-19, and 21-24 are on appeal. Of all pending claims, claims 1, 8, 14 and 21 are independent, whereas the remaining claims are dependent.

IV. STATUS OF AMENDMENTS

An Amendment After Final was submitted to the US Patent and Trademark Office on April 13, 2006. The Amendment After Final was entered as requested in the Request for Continued Examination (RCE) on May 15, 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to four separate features as evidenced by the four independent claims and their respective dependent claims.

Namely, independent claim 1 and dependent claims 2 and 4-7 recite a thin film transistor. Independent claim 8 and dependent claims 9 and 11-13 recite a flat panel display. Independent claim 14 and dependent claims 15 and 17-19 recite a Thin Film Transistor (TFT). Lastly, independent claim 21 and dependent claims 22-24 recites a process for making a flat panel display.

With regard to the thin film transistor, the specific features thereof are discussed in paragraphs [0042]-[0046] and illustrated in Figs. 2 and 7-10.

With regard to the flat panel display, the specific features thereof are discussed in paragraphs [0026]-[0039] and illustrated in Figs. 1-4.

With regard to the TFT, the specific features thereof are also discussed in paragraphs [0042]-[0046] and illustrated in Figs. 2 and 7-10.

Lastly, with regard to the process for making a flat panel display, the specific features thereof are discussed in paragraphs [0042]-[0051].

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims1, 2, 4-7, 9, 14, 15, and 17-19 have been rejected under 35 U.S.C. §103 as obvious over Ohtani *et al.* (U.S. Patent No. 6,271,543) in view of Maeda (U.S. Patent No. 5,278,099) for the reasons stated on pages 2-5 of the Office Action mailed on 9 March 2007 (Paper No. 20070305).

Claims 8-13 and 21-24 have been rejected under 35 U.S.C. §103 as obvious over Ohtani in view of Maeda and Yamazaki *et al.* (U.S. Patent Publication No. 2003/0222575) for the reasons stated on pages 5-7 of the Office Action mailed on 9 March 2007 (Paper No. 20070305).

VII. ARGUMENT

The Examiner has correctly noted that Ohtani et al. teaches a three-layer laminated structure of titanium/aluminum/titanium for the source wiring line and drain electrode of Ohtani et al. (See lines 10-13 of column 7 of Ohtani et al.)

However, lines 59-62 of column 6 of Ohtani et al. indicate that a film of aluminum or a material mainly containing aluminum is formed and patterned to form the gate wiring line of Ohtani et al.

Accordingly, it is submitted that Ohtani et al. teaches away from a three-layer laminated structure of titanium/aluminum alloy/titanium in that there is an inference that Ohtani's failure to indicate that an aluminum alloy can be used for the source wiring line and drain electrode after previously indicating that an aluminum or aluminum alloy can be used for the gate wiring line infers that Ohtani **only** considered pure aluminum for the source wiring line and drain electrode.

Furthermore, while Maeda indicates in lines 22-31 of column 4 thereof that the layer 36 is not limited to pure aluminum but rather can be an aluminum alloy, Maeda indicates in lines a 62-64 of column 3 thereof that since the TiN layer 34 has a thickness sufficient to prevent the growth of alloy spikes, aluminum layer 36 need not contain silicon. Accordingly, there is an inference that the use of a TiN layer precludes the need for an aluminum alloy layer and allows the layer 36 to be pure aluminum.

The independent claims recite that one of the source electrode and drain electrode

comprises an aluminum alloy layer disposed between a pair of titanium layers. That is, the recitation that the gate electrode comprises an aluminum alloy layer disposed between a pair of titanium layers has been deleted.

Ohtani et al., on the other hand, refers to a titanium/aluminum/titanium structure only for the source and drain electrodes and refers to an aluminum alloy only for the gate electrodes. Thus, the source and drain electrodes of Ohtani et al. do not correspond to the recited source and drain electrodes of the independent claims.

In responding to the above-noted arguments contained in the previously submitted September 27, 2005 Amendment and April 13, 2006 Amendment After Final, the Examiner **admits** on page 7 of the July 28, 2006 Office Action that "Ohtani . . . does not specifically disclose that the Al layer is an aluminum alloy layer." The Examiner then continues: "The gate electrode having the same Ti/Al/Ti structure is cited in Ohtani as using an Al layer. Therefore, it is **assumed** that the source and drain electrodes of Ohtani **may** also comprise an Al alloy." (Emphasis added)

Appellants strongly disagree with the Examiner's unsupported assumptions. That is, there is no teaching or suggestion or incentive in Ohtani to fabricate the source and drain electrodes with the same material used to fabricate the gate electrode. In fact, the source and drain electrodes are oftentimes of a different material than that used for the gate electrode.

Furthermore, even assuming arguendo that the source and drain electrodes are of the same material as the gate electrode, this does not result in the conclusion that it would be obvious to

fabricate the source and drain electrodes of the same material as the gate electrode.

Stated simply, it is settled patent law that merely because one **can** modify a subject device in a reference to produce a device which purportedly meets the recited limitations of a rejected claim does **not** mean that it would be obvious to do so. The Examiner has used the wrong criterion to argue the obviousness of modifying a reference.

Furthermore, the Examiner argues that Maeda was cited to cure the deficiencies of Ohtani in that Maeda discloses that an electrode **can** comprise an alloy of aluminum. Again, the Examiner has used the wrong criterion to argue the obviousness of modifying a reference.

As to the recited specific weight percentage of the element in the alloy and the thickness of the titanium nitride layer or the percentage of nitrogen within the desired range, the Examiner has made an unsupported statement that these recited features would be obvious to one skilled in the art. Yet, the Examiner admits that neither Ohtani nor Maeda teaches or suggests these recited features, nor has the Examiner submitted secondary references which teach or suggest these recited features.

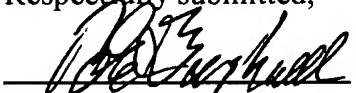
As to the rejection of claim 18, even disregarding the recited process limitation, claim 18 recites that the semiconductor of layer forming a conductive channel between the source electrode and drain electrode upon application of a voltage to the gate electrode does not appear to have been considered by the Examiner.

With regard to the specific comments by the Examiner in rejecting claims 8 and 21, the Examiner admits that Ohtani does not show the complete active-matrix having a second plurality of thin-film transistors, wherein the first drain electrodes of the first plurality of thin-film transistors are electrically connected to gate electrodes of the second plurality of thin-film transistors. The Examiner then argues that such a recitation is that of a well-known routing scheme and then cites the Yamazaki publication as teaching such a feature.

However, the Examiner has only rejected claims 8 and 21 as obvious over the combination of Ohtani and Maeda and the inclusion of the citation of the Yamazaki publication is therefore improper.

In conclusion, it is submitted that it would not be obvious to combine the features of Ohtani and Maeda in the fashion noted by the Examiner such that it is submitted that all of the claims now on appeal are patentable over the combination of Ohtani and Maeda and should now be in a condition suitable for allowance.

Respectfully submitted,



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VIII. APPENDIX

CLAIMS UNDER APPEAL (Claims 1, 2, 4-9, 11-15, 17-19, 21-24)

1. (Previously Presented) A thin film transistor, comprising a source electrode, a drain electrode, a gate electrode and a semiconductor layer, wherein one of the source electrode and drain electrode comprises an aluminum alloy layer disposed between a pair of titanium layers, wherein a diffusion prevention layer is interposed between the aluminum alloy layer and each of the pair of titanium layers, and wherein the aluminum alloy layer comprises at least one element selected from a group consisting of silicon, copper, neodymium, platinum and nickel.

2. (Original) The thin film transistor of claim 1, wherein the aluminum alloy layer comprises about 0.1 to 5 wt% of at least one element selected from a group consisting of silicon, copper, neodymium, platinum and nickel.

4. (Previously Presented) The thin film transistor of claim 1, wherein each diffusion prevention layer is made of titanium nitride.

5. (Previously Presented) The thin film transistor of claim 4, wherein each titanium nitride layer has a thickness between 100 and 500Å.

6. (Previously Presented) The thin film transistor of claim 4, wherein each titanium nitride layer contains 5 to 85 wt% of nitrogen.

7. (Original) The thin film transistor of claim 1, each electrode being absent of pure

aluminum.

8. (Previously Presented) A flat panel display, comprising:

a substrate;

a first plurality of thin film transistors formed on a surface of the substrate, the first plurality of thin film transistors comprising first source electrodes, first drain electrodes, first gate electrodes, and semiconductor layers;

a plurality of first conductive lines electrically connected to the first source electrodes; and

a plurality of second conductive lines electrically connected to the first gate electrodes;

a second plurality of thin film transistors, wherein the first drain electrodes of the first plurality of thin film transistors are electrically connected to gate electrodes of the second plurality of thin film transistors, wherein one of the first source electrodes, the first drain electrodes, the plurality of first conductive lines, and the plurality of second conductive lines comprises an aluminum alloy layer and a titanium layer formed on both surfaces of the aluminum alloy layer, wherein a diffusion prevention layer is interposed between the aluminum alloy layer and the titanium layers, and wherein the aluminum alloy layer comprises at least one element selected from a group consisting of silicon, copper, neodymium, platinum and nickel.

9. (Original) The flat panel display of claim 8, wherein the aluminum alloy layer comprises about 0.1 to 5 wt% of at least one element selected from the group consisting of silicon, copper, neodymium, platinum and nickel.

11. (Previously Presented) The flat panel display of claim 8, wherein each diffusion prevention layer is made of titanium nitride.

12. (Previously Presented) The flat panel display of claim 11, wherein each titanium nitride layer has a thickness between 100 to 500Å.

13. (Original) The flat panel display of claim 11, wherein each titanium nitride layer contains 5 to 85 wt% of nitrogen.

14. (Previously Presented) A TFT, comprising:

a source electrode, a gate electrode and a drain electrode; and

a semiconductor layer between the source electrode and the drain electrode, wherein one of said source electrode and said drain electrode contain an aluminum alloy layer bounded by a pair of titanium layers and not a pure aluminum layer, wherein said source electrode and said drain electrode each comprising a TiN diffusion prevention layer between the aluminum alloy layer and each titanium layer, and wherein the aluminum alloy layer comprises at least one element selected from a group consisting of silicon, copper, neodymium, platinum and nickel.

15. (Original) The TFT of claim 14, wherein the aluminum alloy layer comprises about 0.1 to 5 wt% of at least one element selected from the group consisting of silicon, copper, neodymium, platinum and nickel.

17. (Original) The TFT of claim 14, said semiconductor layer being absent of aluminum after said TFT is subjected to a heat treatment of at least 300 degrees Celsius.

18. (Original) The TFT of claim 14, said semiconductor layer being primarily made of silicon and said semiconductive layer forming a conductive channel between said source electrode and said drain electrode upon application of a voltage to the gate electrode after said TFT is exposed to heat of at least 300 degrees Celsius.

19. (Original) The TFT of claim 14, said source electrode and said drain electrode both being formed of aluminum alloy and both being absent pure aluminum.

21. (Previously Presented) A process for making a flat panel display, comprising:

forming a first plurality of thin film transistors formed on a surface of a substrate, the first plurality of thin film transistors comprising first source electrodes, first drain electrodes, first gate electrodes, and semiconductor layers;

electrically connecting a plurality of first conductive lines to the first source electrodes;

electrically connecting a plurality of second conductive lines to the first gate electrodes; and

forming a second plurality of thin film transistors, electrically connecting the first drain electrodes of the first plurality of thin film transistors to gate electrodes of the second plurality of thin film transistors, wherein one of the first source electrodes, the first drain electrodes, the plurality of first conductive lines, and the plurality of second conductive lines comprises an aluminum alloy layer and a titanium layer formed on both surfaces of the aluminum alloy layer, and interposing a diffusion prevention layer between the aluminum alloy layer and the titanium layers, and wherein the aluminum alloy layer comprises at least one element selected from a group consisting of silicon, copper, neodymium, platinum and nickel.

22. (Previously Presented) The process of claim 21, comprised of making the aluminum alloy layer from an aluminum alloy comprising about 0.1 to 5 wt% of at least one element selected from the group consisting of silicon, copper, neodymium, platinum and nickel.

23. (Previously Presented) The process of claim 21, comprised of making the diffusion prevention layers of titanium nitride.

24. (Previously Presented) The process of claim 23, comprised of making the titanium nitride layers with a thickness between 100 to 500Å.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.